

Remarks

Claims 1-17, 21, and 23-25 are pending. Reconsideration of claims 1-17, 21, and 23-25 is requested.

Claims 1, 3-5, 12-14, 16-17, 21, and 23-24 stand "rejected under 35 U.S.C. §102(b) as being anticipated by Wu et al., US patent No. 6,013,581." OFFICE ACTION, July 31, 2006, p. 2.

Wu et al. explicitly teaches a glue layer "208" sandwiched between and in contact with a pair of dielectric layers "206" and "210", as best shown in Fig. 2E of U.S. Pat. No. 6,013,581. As shown in FIG. 2E, a portion of the glue layer "208" is in contact with a barrier/glue layer "222" rather than dielectric layer "210". In either case, the structure described by Wu et al. does not include a metal layer deposited "directly onto the upper surface of [an] inter-treated glue layer," as recited, in part, in claim 1. Also, a method of manufacturing the structure disclosed by Wu et al. does not include "forming a metal layer directly on the upper surface of [a] glue layer," as recited, in part, in claim 12. Regarding claim 21, the method of manufacturing the structure disclosed by Wu et al. does not include "forming a second metal layer directly on the upper surface of [a] glue layer," as recited, in part, in claim 21.

In sustaining the rejection of claims 1, 3-5, 12-14, 16-17, 21, and 23-24, the Examiner reiterated that "the limitation of the metal layer being formed on the upper surface of the inter-treated glue layer does not imply that the metal layer is formed directly on the inter-treated glue layer." OFFICE ACTION, July 31, 2006, p. 11. Accordingly, claim 1 has been amended to call for "the second layer" to be deposited "directly onto the upper surface of the inter-treated glue layer." Claim 12 has been amended to call for forming a metal layer "directly on" the upper surface of the glue layer. Also, claim 21 has been amended to call for a "second metal layer" being formed "on" the upper surface of the glue layer such that an interface is formed directly between metal of the second metal layer and the upper surface of the glue layer." As such, claims 1, 12, and 21, as well as those claims depending therefrom, are in condition for allowance.

Claim 25 stands "rejected under 35 U.S.C. §102(b) as being anticipated by Dixit et al., US patent No. 6,355,558." OFFICE ACTION, July 31, 2006, p. 6. Dixit discloses "[a]

metallization structure, and associated method, for filling contact and via apertures to significantly reduce the occurrence of microvoids and provide desirable grain orientation and texture." Abstract. The metallization structure, as shown in the FIG. 2F, reproduced below, includes a wetting or glue layer 42, a barrier layer 44 atop the wetting layer, a refractory metal layer 46 atop the barrier layer, and an aluminum layer 48 atop the metal layer 46. The Examiner

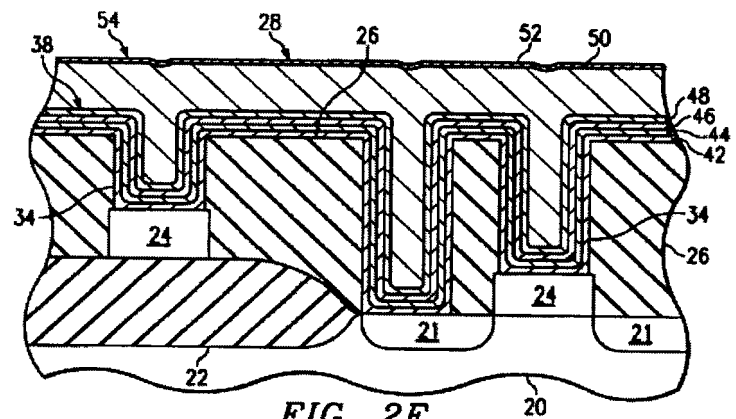
has concluded that this multi-layered construction anticipates that recited in claim 25. Specifically, the Examiner has asserted that layer 42 is "a first metal layer". However, Dixit et al. describes layer 42 as a wetting or glue layer.

Moreover, even assuming that the glue layer constitutes a metal layer, Dixit et al. teaches that a barrier layer is deposited on

layer 42. The barrier layer is not a glue layer. The reference teaches that the barrier layer "acts as a barrier material in order to stop or inhibit interaction between the subsequent metallization deposited and the underlying silicon." Col. 4, lns. 43-45. Thus, Dixit et al. discloses that a barrier is formed between layer 42 and layer 48, but does not disclose that a layer of adhesion is formed therebetween.

Furthermore, even assuming that the barrier layer constitutes a glue layer, Dixit et al. discloses that "an optional barrier fortification step [is] performed to 'stuff' the barrier layer to improve the performance of the barrier layer to keep the subsequently deposited Al from diffusing, or spiking, through the barrier layer into the underlying silicon." Col. 4, lns. 52-56. Thus, the reference teaches a step for improving the blocking performance of the barrier layer – not for improving any adhesiveness of the layer.

Therefore, Dixit et al. fails to teach or suggest "a method for improving an interface in a semiconductor device" that includes "forming a first metal layer; forming a glue layer directly on



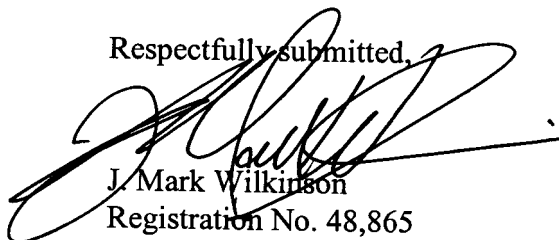
the first metal layer; performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer for improved adhesiveness; and forming a second metal layer on the upper surface of the glue layer," as called for in claim 25.

Regarding the rejections of claims 2 and 6-11, Applicant respectfully disagrees with the Examiner with respect to the art as applied, but in light of claims 2 and 6-11 depending from what are believed otherwise allowable claims, Applicant does not believe that additional remarks are necessary and requests allowance of claims 2 and 6-11 at least pursuant to the chain of dependency.

Therefore, it is clear from at least the foregoing that independent claims 1, 12, 21, and 25 are patentably distinct from that disclosed by the art of record and, therefore, are in condition for allowance. Dependent claims 2-11, 13-17, 23, and 24 depend from and further limit independent claims 1, 12, and 21 and therefore are allowable as well.

As no outstanding issues remain, an early formal notice of allowance of claims 1-17, 21, and 23-25 is requested.

Respectfully submitted,



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Dated: 10-3-06
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Docket Number: 2002-0893 / 24061.220
R-143437_1.DOC